

Variant 005 (fully populated) shown. For block diagrams of other Variants, refer to the TIDA-01480 Design Guide (TIDUDN1)

Revision History

Rev	ECN #	Approved Date	Approved by	Notes
E1	N/A	2017-11-14	Brian Berner	1st Build
E2	N/A	2017-12-06	Brian Berner	1st Web Release

A

B

C

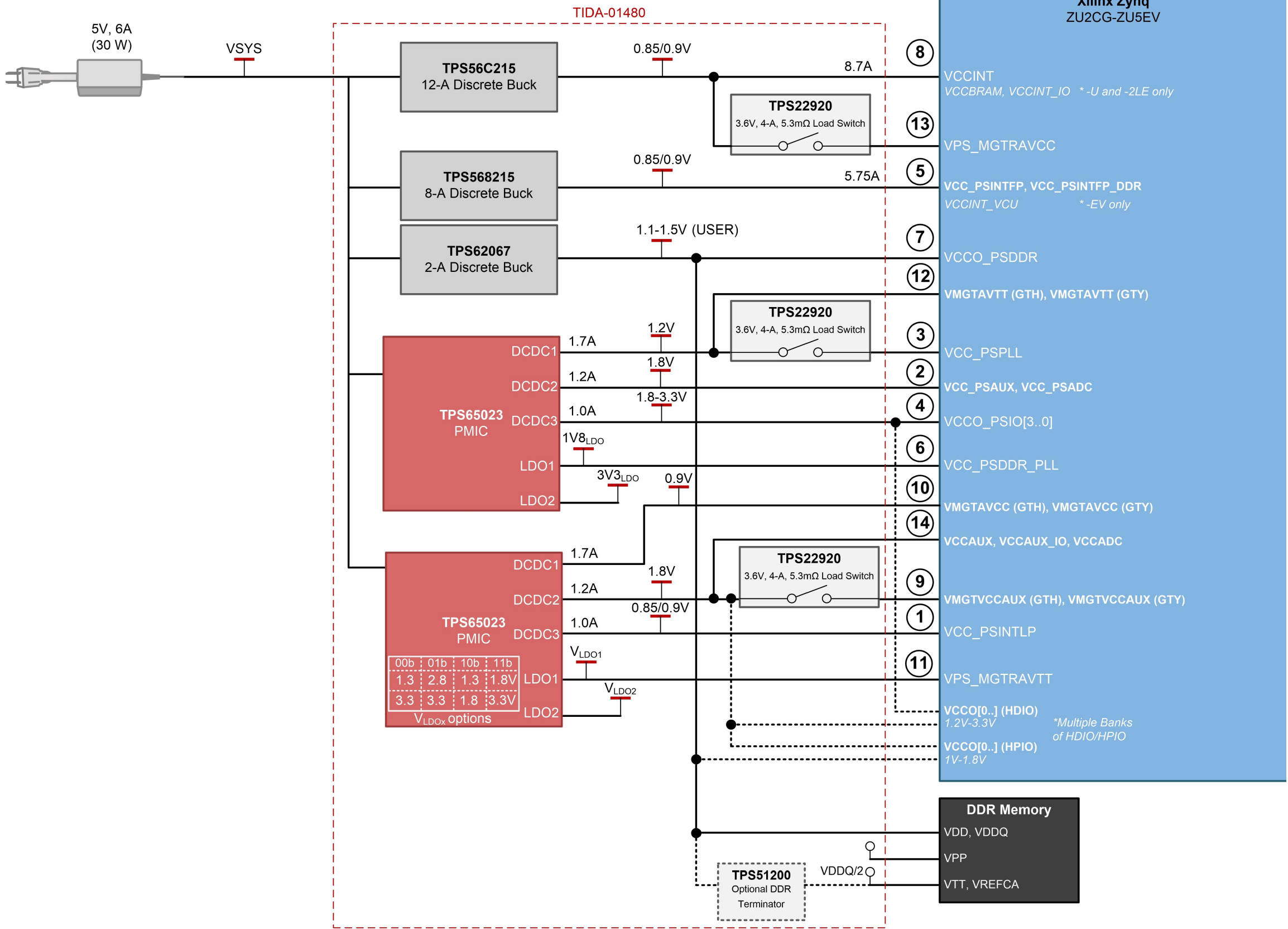
D

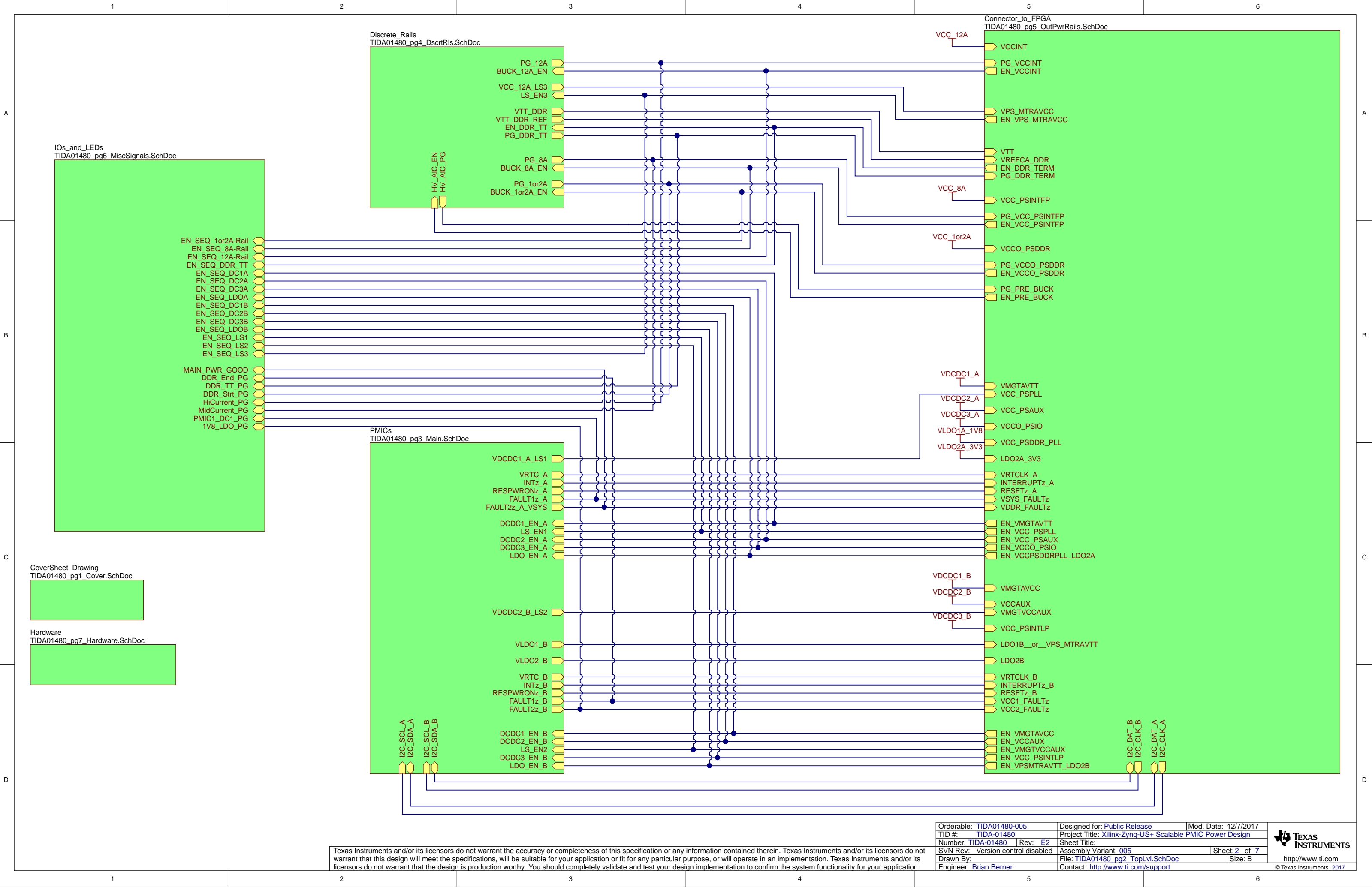
A

B

C

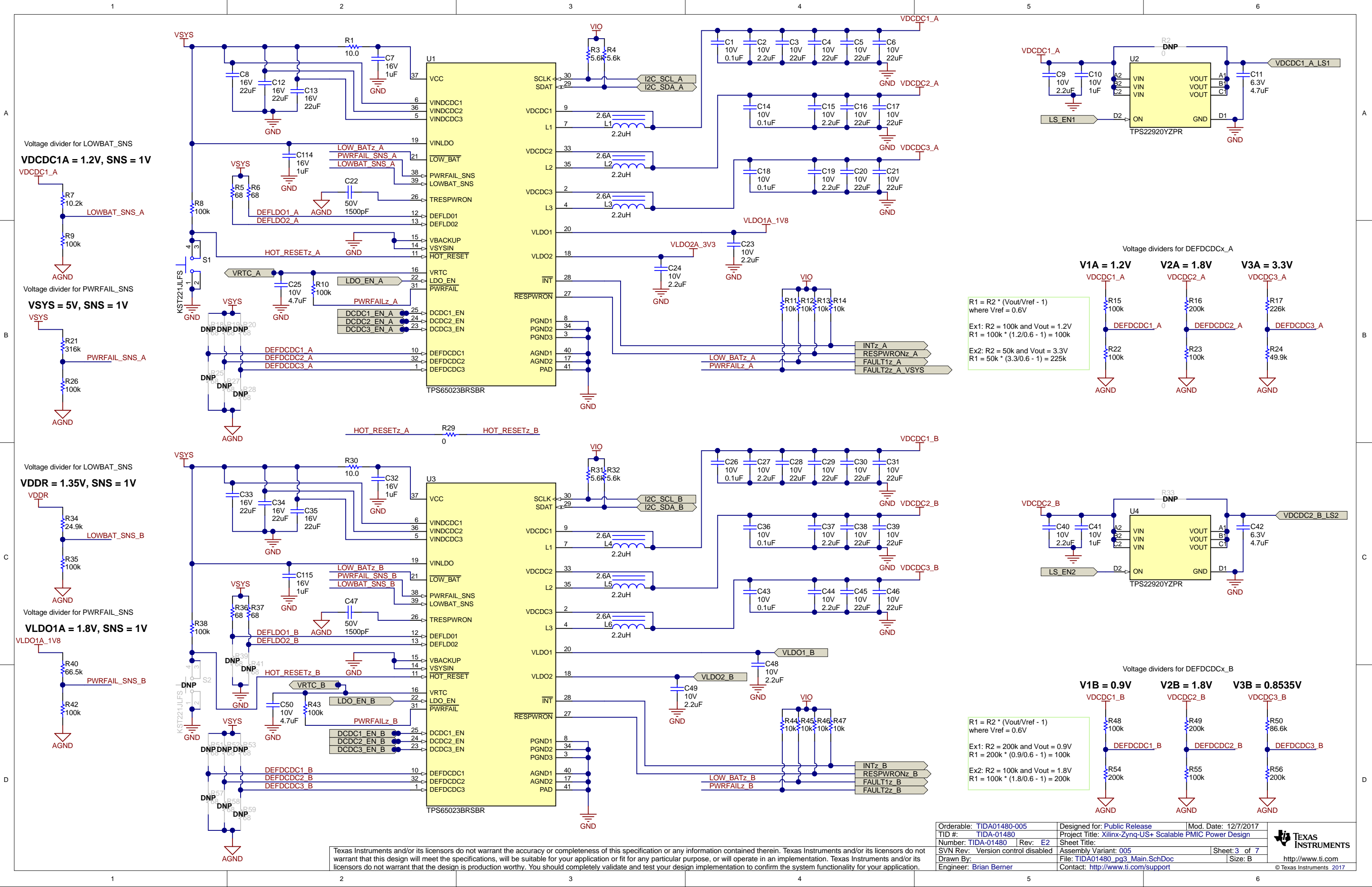
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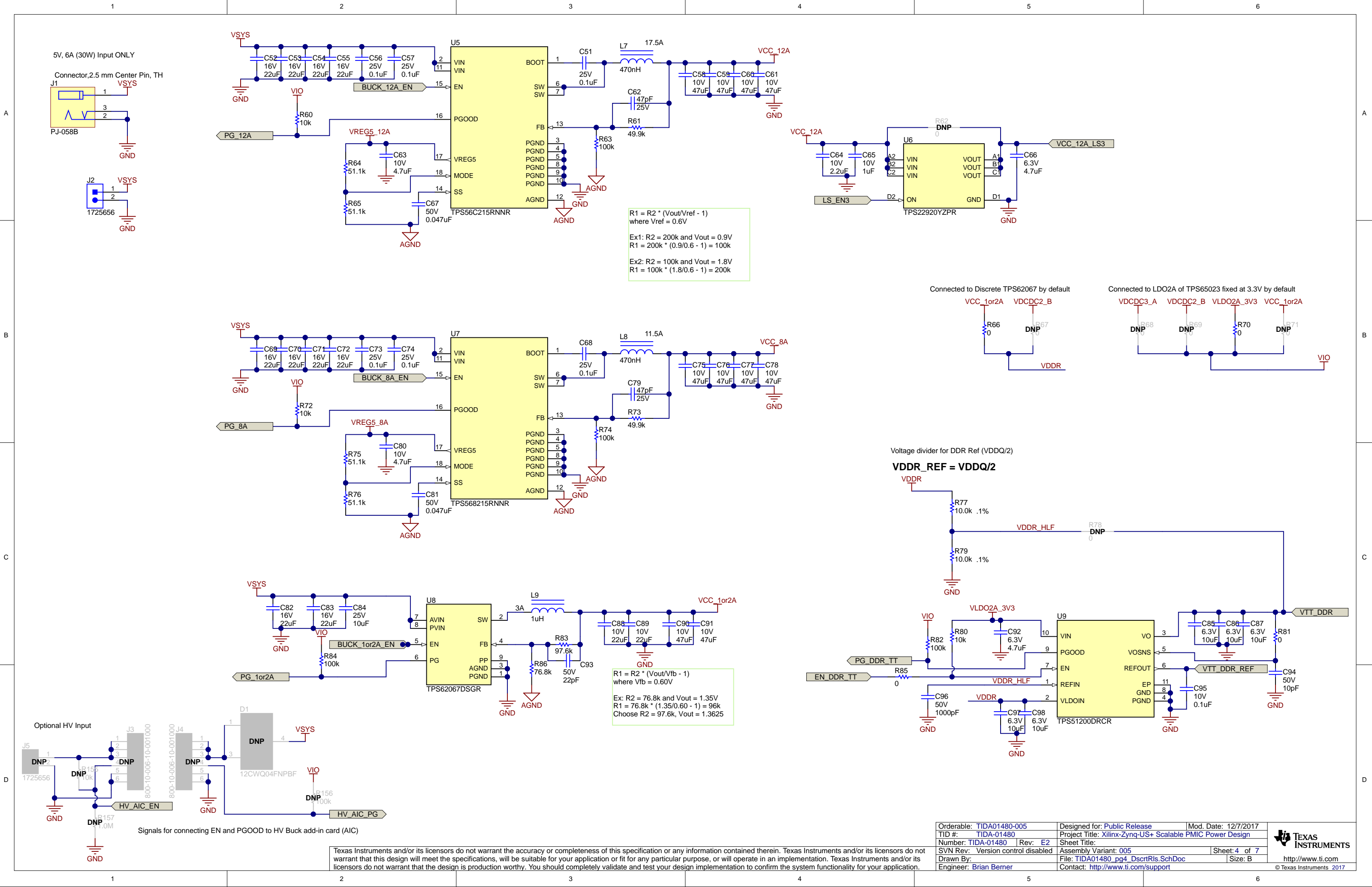


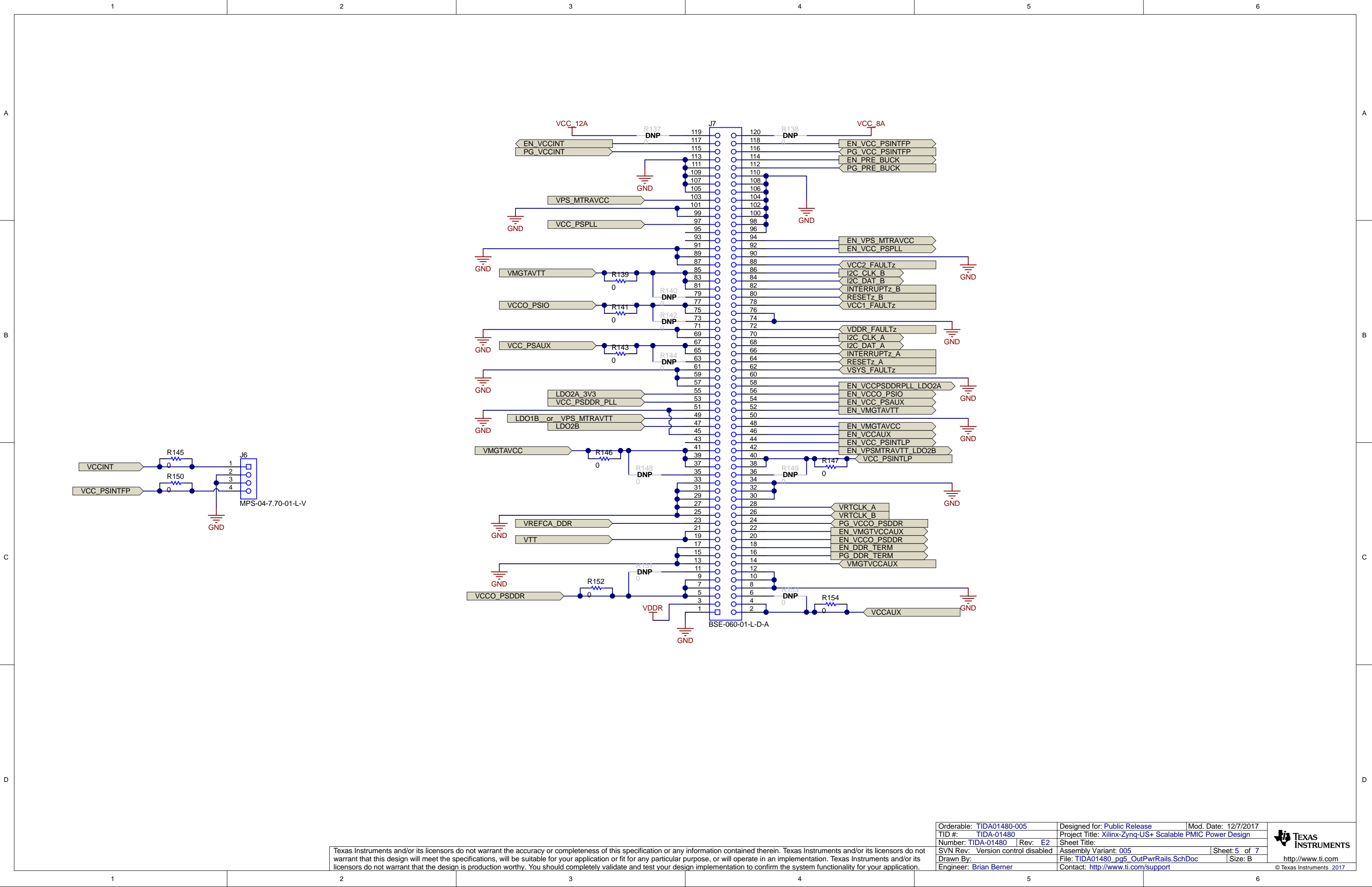


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Orderable: TIDA01480-005	Designed for: Public Release	Mod. Date: 12/7/2017
TID #: TIDA-01480	Project Title: Xilinx-Zynq-US+ Scalable PMIC Power Design	
Number: TIDA-01480	Rev: E2	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 005	Sheet: 2 of 7
Drawn By:	File: TIDA01480_pg2_TopLv1.SchDoc	Size: B
Engineer: Brian Berner	Contact: http://www.ti.com/support	







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TID #: TIDA-01480	Project Title: Xilinx-Zynq-US+ Scalable PMIC Power Design	
Number: TIDA-01480	Rev: E2	Sheet Title: Assembly Variant: 005
SVN Rev: Version control disabled	File: TIDA01480_pg5_OutPwrRails.SchDoc	Sheet: 5 of 7
Drawn By: Brian Berner	Contact: http://www.ti.com/support	Size: B
Engineer: Brian Berner		

